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DESIGN AND OPTIMIZATION OF REVERSIBLE CARRY LOOK AHEAD ADDER CIRCUIT

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ABSTRACT

Power dissipation is a prominent factor in limiting the chip area. Conventional computing has been facing many challenges from the last couple of decades. The device scaling versus technology has reached saturation, forcing the designers to look for alternative methods. Reversible design is a promising alternative to these limitations, with increasing applications such as nano-computing, quantum computing, low power dissipating digital designs, etc. Reversible logic promises the minimization or even elimination of power dissipation [1][2][3]. In this paper, the Carry Look-ahead Adder (CLA) circuit is designed using reversible logic. The proposed deigns are efficient compared to the existing designs in terms of gate counts, garbage outputs and quantum cost. The design can be extended to construct an n-bit adder circuit. Extension to a 16 bit adder is also shown in this paper. The results given in the paper show that the reversible designs dissipates very less power than the CMOS design. The 16-bit CLA using Toffoli gates dissipated 0.21% and design using Peres gates dissipated 0.27% compared to the power dissipated by conventional CMOS design.

KEYWORDS: Reversible Logic, Constant/Garbage Input, Garbage Output, Quantum Cost, CLA

INTRODUCTION

Power dissipation is the most limiting factor in VLSI designs. At the least, the combinational circuits dissipate KTln2 joules [1] for every information bit erased, where K = $1.3806505 \times 10^{-23}$ J/K is Boltzmann constant and T is the absolute operating temperature. By Moore's law, number of transistors doubles approximately every two years [1][2]. As number of transistors increases, the power dissipation also increases [4].

Charles Bennett showed that power dissipation could be avoided or even eliminated by reversible logic [1]. He also proved that circuit built from reversible gates have zero power dissipation. In reversible gates, there is unique mapping between the inputs and outputs, unlike in conventional logic. Reversible gates are used in quantum computing system since quantum operations are reversible in nature. The reversible circuit/gates are characterized by: (i) Equal number of inputs and outputs (ii) Garbage outputs (iii) Number of constant/garbage inputs (iv) The fan-out of each gate which is equal to one (A copying circuit is used to increase fan out).

Efficient reversible logic design dictates [3]: (a) use minimum reversible logic gates (b) Minimal garbage outputs (c) less constant inputs and (d) minimization of quantum cost. Addition operation is the most widely used arithmetic operation. Even multiplication is described as successive addition, which is used in almost every ALU. Thus a Low power, Low cost adder circuit is very much in need, to meet the demanding requirements.

INTRODUCTION TO LOW POWER ADDERS

Carry Skip Adder (CSA)

In this technique, the (n) bits are divided into (P) groups of equal (k) bits with k1 as block delay. Propagate signals are generated in each blocks. If the group propagate signal is high, then the carry skips the entire block. Figure 1 shows the block diagram of a 16 bit CSA:

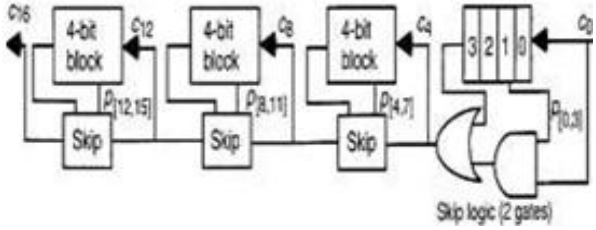

Figure 1: 16 Bit CSA

If the CSA is to have M multiplexers with delay of k2, then the total worst case delay is given by

T = 2 (P - 1) k1 + (M - 2) k2.

Where M = √ ((2 n k1) / k2)

For n = 16 and assuming k1=k2=k, T can be approximated to 7k s.

N-Bit Carry Select Adder

The adder consists of one n/2 – bit adder for the lower half of the bits and two n/2-bit adders for the other half of the bits. In the latter part of addition, one part performs with Cin=0 assumption and the other part works with Cin=1 assumption. The final carry is selected by the use of multiplexers. This technique does use increased area, but also speeds up the addition operation. The architecture of the adder is shown in Figure 2.

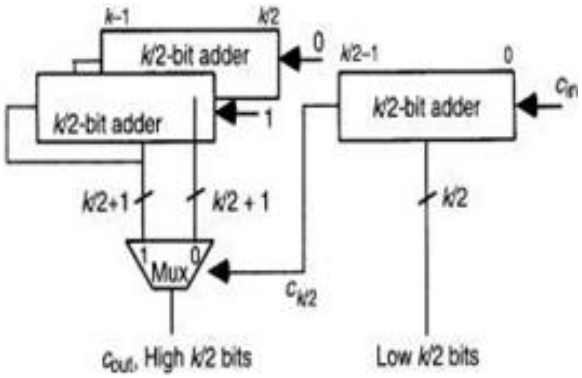

Figure 2: Carry Select Adder

Let the n bit adder be divided into M blocks with P adder cells. If k1 is the delay through one adder cell and k2 is the delay through multiplexer in next block, then the latency through the adder is

T = P k1 + (M – 1) k2.

Where M = √ (n k1 / k2).

For n = 16 and assuming k1=k2=k, T can be approximated to 7k.

Carry Look Ahead Adder (CLA)

Carry Look Ahead addition is based on the fact that a carry signal will be generated if:

- Both bits A and B are 1, or
- One of the two bits is 1 and the carry-in (carry of the previous stage) is 1.

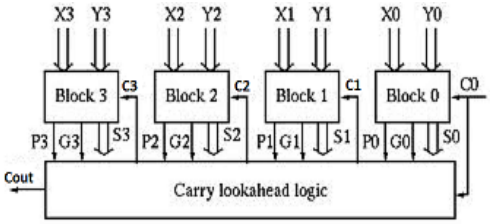

Figure 3: 1 Block CLA

The Boolean expression of the carry outputs(C*) of various stages can be written as follows:

C1 = G0 + P0C0

C2 = G1 + P1C1 = G1 + P1 (G0 + P0C0)

= G1 + P1G0 + P1P0C0

C3 = G2 + P2C2

= G2 + P2G1 + P2P1G0 + P2P1P0C0

C4 = G3 + P3C3

= G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C0

Where G = AB and P= A XOR B.

IMPORTANT REVERSIBLE GATES

Toffoli Gate

The 3*3 gate has inputs (A, B, C) mapped to the outputs (P = A, Q = B, R = A.B XOR C) is shown in Figure 4.

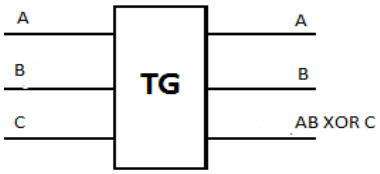

Figure 4: TOFFOLI Gate

Quantum Implementation is as shown in Figure 5

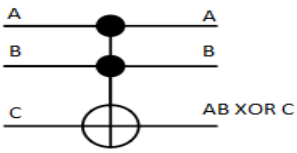

Figure 5: Quantum Implementation

Peres Gate

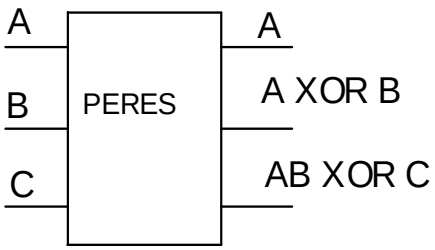

Figure 6: PERES Gate

The 3*3 Reversible gate with inputs (A, B, C) mapped to outputs (P = A, Q = A XOR B, R = (A.B) XOR C). The Peres gate quantum implementation is shown in Figure 7

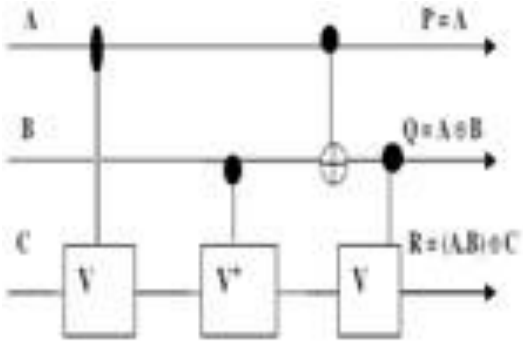

Figure 7: Quantum Implementation of PERES Gate

DESIGN AND WORK

- **Design Using Conventional CMOS Logic**

The generate and propagate blocks for a 4 bit CLA and a 16 bit ripple CLA was realized first using conventional CMOS logic. The simulation was done in Cadence Virtuoso and H Spice using 90 nanometer technology.

The total source power dissipation was found to be 5.1255nW for the 4 bit CLA and 3.805uW for the 16 bit RIPPLE CLA.

- **Design Using Reversible Logic**

The reversible CLA was designed and implemented in two ways: 1. Using Toffoli gates, 2. Using Peres gates. The reversible designs were implemented using pass transistor logic. External power supply was not used in both the designs. The whole circuit was made to run on just the inputs. The simulation was done both in Virtuoso and H Spice tools, using 90nm MOSFET model files.

- **Design Using Toffoli Gates**

The REVKIT implementation of a 4-bit Toffoli CLA is as shown in Figure 8

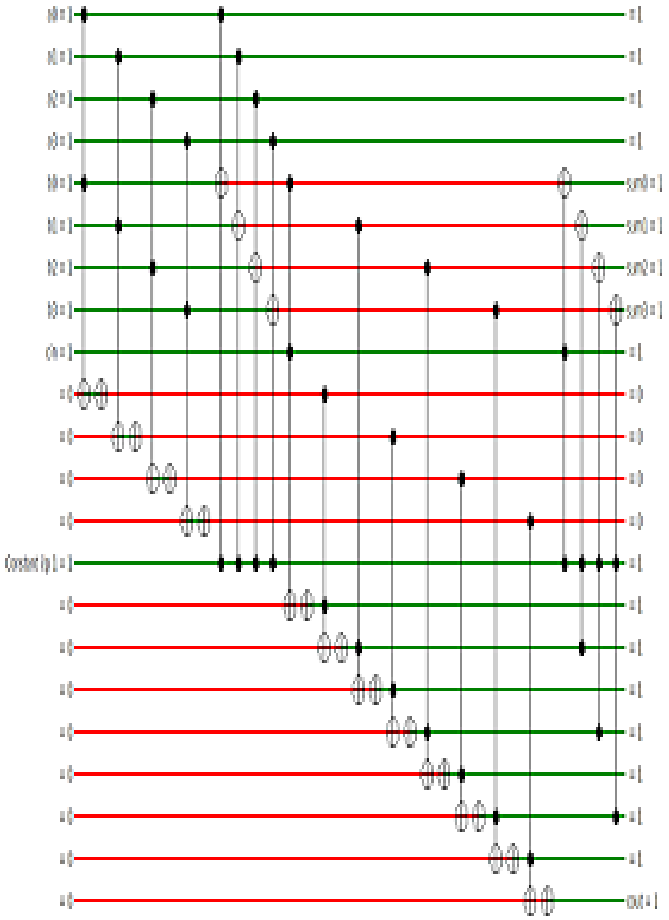

Figure 8: REVKIT Implementation of TOFFOLI CLA

The whole design was then implemented using pass transistor logic. Here HSpice and Cadence Virtuoso was used to simulate the design in 90nm technology.

The Parameters observed in the designs were:

Table 1: Parameters for Toffoli Design

Parameter	4 Bit	Ripple CLA
Quantum Cost	112	448
Gate Cost	32	128
Transistor Cost	320	1280
Line Cost	22	88
Power Dissipation	2.586nW	7.852nW

- **Design Using Peres Gate**

The REVKIT implementation of a Peres CLA is as shown in Figure 9.

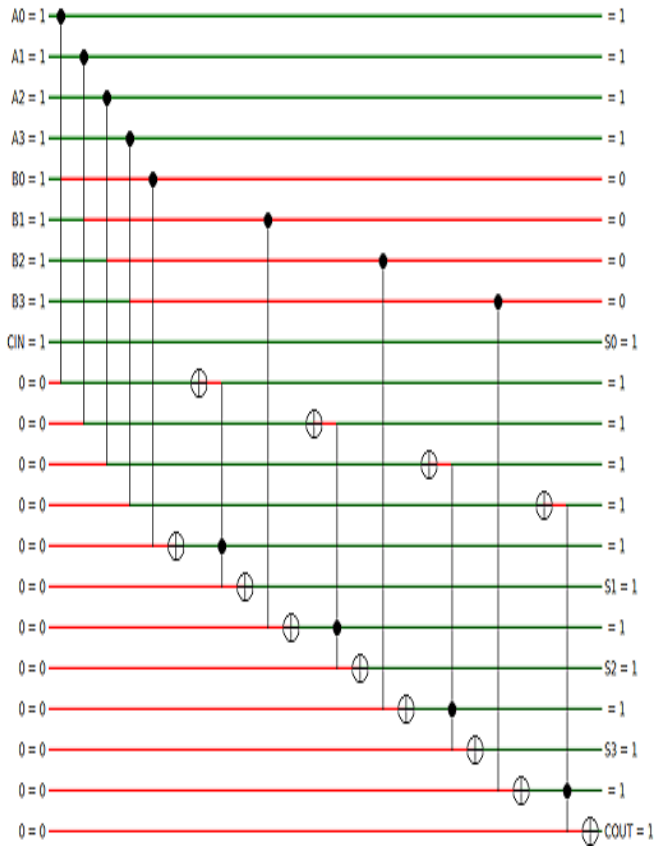

Figure 9: REVKIT Implementation of PERES CLA

Table 2: Parameters for Peres Design

Parameter	4 Bit	Ripple CLA
Quantum Cost	24	96
Gate Cost	24	96
Transistor Cost	96	384
Line Cost	21	84
Power Dissipation	2.586nW	10.345nW

The above design was then implemented using pass transistor logic. Here HSpice and Cadence Virtuoso was used to simulate the design in 90nm technology.

COMPARISON

The comparison between various design parameters for all designs implemented in this paper is as follows:

Table 3: Design Comparison

PARAMETER	CMOS CLA(4 |16 Bit)		TOFFOLI CLA		PERES CLA	
Power Dissipation	**5.1255nw**	**3.805uw**	**2.586nw**	**7.852nw**	**2.586nw**	**10.345nw**
Gate cost	-		32	128	24	96
Transistor Cost	-		320	1280	96	384
Quantum Cost	-		112	448	24	96
Line Cost	-		22	88	21	84

The reversible designs on average dissipate 0.23% of power dissipated by the conventional design. The Toffoli design is 24% more efficient than the Peres design in terms of power dissipation but the Peres design is more efficient in terms of gate cost, transistor cost and quantum costs, as shown in the table.

CONCLUSIONS

The conventional design dissipated 5.125 nw in 4 bits and 3.80uw in the 16 bits mode whereas the reversible designs dissipated less power by a factor of 400 for the Toffoli and a factor of 300 for the Peres design. The comparatively less dissipation of power by the reversible designs can be attributed to the non-usage of external power supplies. The Peres gates design was superior to that by Toffoli in terms of gate costs, transistor costs and quantum costs. The Toffoli gates design achieves 24% optimization in terms of power dissipation, than the Peres design but at the cost of Quantum costs and transistor costs.

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